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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/654,760	05/29/96	VORA M	V&F-001

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EXAMINER	
GIORDANA,A	
ART UNIT	**PAPER NUMBER**
2512	

DATE MAILED: 07/15/97

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)
*U.S. GPO: 1997-422-198/60031

1- File Copy

Office Action Summary

Application No.	Applicant(s)
08/654,760	Vora
Examiner	**Group Art Unit**
Adriana Giordana	2512

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1 and 2* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1 and 2* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Drawings

1. Figures 3 and 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Specification

2. The disclosure is objected to because of informalities; for example, on page 1, line 11, "appliction" should read "application".

Appropriate correction is required.

Claim Objections

3. Claim 1 is objected to because of the following informalities: on line 8, "flaotign" should read "floating". Appropriate correction is required.

Claim Rejections - 35 U.S.C. § 112

4. Claims 1-2 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 4, it is unclear how the layers "intersect" the well, as to intersect can mean "to cut through or across," while the drawings clearly show the layers as external to the well; on line 6, the "materials" lack antecedent basis.

In claim 2, lines 2-9, the relationship between the conductivity types is unclear, as for example it is unclear if the "a first conductivity types" of lines 2 and 8-9 are meant to be the same, and if the "second conductivity type" of lines 3-4 is meant to differ from the "first conductivity type; on line 4, it is unclear if the "layer" or the "conductivity type" is "suitable to act;" furthermore, it is unclear if the "layer" or the "conductivity type" does actually act as a channel region, as conceivably every semiconductor layer could act as a channel of a transistor, but does not necessarily do so; on line 26, it is unclear if the "second layer of insulating material" is the same as the "second insulating layer" of line 16.

Claim Rejections - 35 U.S.C. § 102/103

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that

the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 1 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Mori.

Mori discloses a non volatile memory cell 20 (Figs. 1a-1b) comprising: a semiconductor substrate 11; a vertical MOS transistor formed by alternating N-type and P-type doped layers 32, 36, and 34 in said substrate, and a well 22 etched (col. 8, lines 46-52) into the substrate and penetrating the doped layers; the well having a floating gate FG formed therein and insulated from the doped layers by gate oxide GO; a word line contact PG (col. 9, lines 51-53) comprising a layer of conductive material (col. 9, lines 37-44) extending into the well and overlying the floating gate being insulated from it by layer ILO. Mori also discloses bit lines BL extending along directions perpendicular to the word lines WL (Fig. 3). A bit line contact 34a comprising a layer of conductive material in contact to drain layer 34 is assumed inherent to Mori's disclosure, as Mori shows an opening in insulating layer GO for said contact (col. 5, lines 35-37, and Fig. 1a), and such contact is necessary for the proper functioning of the device.

Should Applicant assert that Mori does not explicitly show the bit line contact, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the device with a bit line contact to the transistor drain extending into opening 34a disclosed by Mori. The rationale is as follows: one of ordinary skill in the art at the time the invention was made would

have been motivated to do so as such bit line contact was necessary for the operation of the memory cell.

Claim Rejections - 35 U.S.C. § 103

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori.

Mori's disclosure is discussed above. It is noted that layer GO can be visualized as having different components covering the bottom and sides of the well, and that the floating gate FG overlies the intersection of the well with buried layer 36, buried layer 36 having opposite conductivity type than regions 32 and 34. It is noted that in Mori's disclosure the portion of substrate 11 below layer 32 does not perform any function beside supporting the device.

Mori does not disclose the substrate having opposite conductivity type than the channel layer, or a second layer of insulating material formed over the word line.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to select the substrate to have the same conductivity type as regions 32 and 36, so that the source, drain, and channel of the transistor would have the same conductivity but could be formed with a single implantation process forming layer 36. The rationale is as follows: one of ordinary skill in the art at the time the invention was made would have been motivated to do so to simplify the manufacturing process of the device. It is noted that such a modification would not affect the operation of the device. It would have been further obvious to one of ordinary skill in the art at the time the invention was made to form a second insulating layer over the word line prior to formation of the bit line as

a necessary process step subsequent to the process step shown in Mori's Figs. 1a-1b. The rationale is as follows: one of ordinary skill in the art at the time the invention was made would have been motivated to do so to isolate the word lines from the bit lines, as said lines overlap as shown in Mori's Fig. 3 and their isolation is necessary for the proper function of the device.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patents 4,964,080 by Tzeng and 5,386,132 by Wong are cited to show memory devices comprising vertical MOS transistors with floating gates and word lines in a well.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adriana Giordana whose telephone number is (703) 308-1293 and whose fax number is 703-308-7722. Any inquiry of a general nature or relating to the status of this application should be directed to the Main Desk whose telephone number is (703) 305-3900.

STUART S. LEVY
SUPERVISORY PATENT EXAMINER
GROUP 2500

Adriana Giordana

July 10, 1997